Teaching Guide				
Identifying Data				2017/18
Subject (*)	Digital Electronics		Code	770G01023
Study programme	Grao en Enxeñaría Electrónica Industrial e Automática			
Descriptors				
Cycle	Period	Year	Type	Credits
Graduate	1st four-month period	Third	Obligatoria	6
Language	Spanish			
Teaching method	Face-to-face			
Prerequisites				
Department	Enxeñaría Industrial			
Coordinador	Meizoso López, Maria del Carmen	E-mail	carmen.meizoso@udc.es	
Lecturers	Meizoso López, Maria del Carmen	E-mail	carmen.meizoso@udc.es	
Web				
General description	Nesta materia preséntanse os fundamentos dos sistemas dixitais. Preténdese que o alumno adquira capacidade para analizar e deseñar circuítos combinacionales e secuenciales. Simboloxía, esquemas e deseño e simulación mediante VHDL.			

Study programme competences	
Code	Study programme competences
A26	Coñecer os fundamentos e aplicacións da electrónica dixital e microprocesadores.
A29	Capacidade para deseñar sistemas electrónicos analóxicos, dixitais e de potencia.
A30	Coñecer e ser capaz de modelar e simular sistemas.
B1	Capacidade de resolver problemas con iniciativa, toma de decisións, creatividade e razoamento crítico.
B2	Capacidade de comunicar e transmitir coñecementos, habilidades e destrezas no campo da enxeñaría industrial.
B3	Capacidade de traballar nun contorno multilingüe e multidisciplinar.
B4	Capacidade de traballar e aprender de forma autónoma e con iniciativa.
B5	Capacidade para empregar as técnicas, habilidades e ferramentas da enxeñaría necesarias para a práctica desta.
B6	Capacidade de usar adecuadamente os recursos de información e aplicar as tecnoloxías da información e as comunicacións na enxeñaría.
B7	Capacidade para traballar de forma colaborativa e de motivar un grupo de traballo.
C3	Utilizar as ferramentas básicas das tecnoloxías da información e as comunicacións (TIC) necesarias para o exercicio da súa profesión e para a aprendizaxe ao longo da súa vida.

Learning outcomes			
Learning outcomes	Study programme competences		
Distingue as distintas familias lóxicas e os tipos de dispositivos dixitais	A26	B1	C3
Deseña circuítos dixitais combinacionales	A29	B2	
Deseña circuitos dixitais secuenciales.	A30	B3	
Aplica as técnicas de análises e simulación de circuítos electrónicos dixitais.		B4	
		B5	
		B6	
		B7	

Contents	
Topic	Sub-topic
Subject 1. Introduction to the Digital Electronics.	Introduction to the Digital Electronics. Number systems and digital codes. Boole´s algebra. Truth tables. Logic gates. Simplification of logic functions.

Subject 2. Introduction to VHDL.	Introduction to the VHDL hardware description language. VHDL basic syntax. Entity. Architecture. Types of data and objects. Operators. Concurrent and sequential sentences: When..else, With..select. Process. Wait, If..then..else, Case...when, For...loop. Components instantiate. Simulation. Test benchs.
Subject 3: Combinational systems.	Technology of digital circuits. Decoders. Coders. Multiplexers. Demultiplexers. VHDL description .
Subject 4: Combinational arithmetic systems	Comparators. Parity circuits. Arithmetic circuits. VHDL description.
Subject 5: Sequential systems.	Latches and Flip-Flops asynchronous and synchronous. Counters. Shift registers. VHDL description.
Subject 6. Memories	Subject 6. Memories. Introdution. Memory types. Memory organization. Read Only Memories (ROM): Internal structure. Types. Control inputs and timming. Aplications. Random Access Memories (RAM):SRAM, DRAM. Internal structure. Timming.
Resumo de contidos segundo a memoria do título: . Introdución á electrónica dixital (Tema 1) · Puertas e funcións booleanas (Tema 1) · Realización electrónica de funcións dixitais (Tema 1) · Bloques dixitais combinacionales (Temas 3 e 4) · Biestables, rexistros e contadores (Tema 5) · Deseño de circuítos dixitais secuenciales: grafos de estados (Tema 5) · Deseño de sistemas dixitais a nivel de bloques (Tema 2) · Tecnoloxías de circuítos integrados dixitais (Tema 3) · Técnicas de análises e simulación de circuítos electrónicos dixitais (Temas 1 e 2)	

Planning				
Methodologies / tests	Competencies	Ordinary class hours	Student?s personal work hours	Total hours
Guest lecture / keynote speech	A26 A29 A30	21	30	51
Problem solving	B1 B5 B7 C2 C3	10	24	34
Laboratory practice	B3 B4 B6 C3	20	22	42
Practical test:	A29 A30	3	8	11
Objective test	B2	2	9	11
Personalized attention		1	0	1
(*)The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.				

Methodologies	
Methodologies	Description
Guest lecture / keynote speech	O profesor guía aos alumnos aclarando os principais conceptos.
Problem solving	Resolvense problemas ou exercicios propostos na aula ou da bibliografía. Pretendese que cada alumno realice un traballo previo a sesión na clase de forma individual.
Laboratory practice	Son sesions obrigatorias para todos os alumnos. Consistirán no deseño e simulación de circuitos dixitais. Requiren preparación previa antes da sesión no laboratorio, con un análise e deseño xustificado da solución adoptada en cada caso. O profesor revisará o traballo previo realizado así como o desenvolvemento na sesión de prácticas.
Practical test:	Consiste no deseño e simulación en VHDL de circuitos dixitais.
Objective test	A proba consistirá en cuestions teórico-prácticas e problemas sobre o contido do curso.

Personalized attention	
Methodologies	**Description**
Guest lecture / keynote speech Problem solving Laboratory practice	The professors will attend personally to the doubts on any of the activities developed throughout the course. The schedule of tuitions will be published at the beginning of the four months on the web page of the center.

Assessment			
Methodologies	**Competencies**	**Description**	**Qualification**
Practical test:	A29 A30	Consiste no deseño e simulación de circuitos dixitais en VHDL utilizando ol software do Laboratorio.	60
Objective test	B2	There will be 3 partial proofs to realize individually by each student. The first will realize once explained the 3 first subjects. It will suppose a 15% of the final grade. The second proof will realize once explained the subjects 4 and 5. It will suppose a 15% of the final grade. The third proof will realize coinciding with the final examination of the 1ª opportunity. This proof will suppose a 20% of the final grade.	40

Assessment comments
The scores for the evaluable tasks are only valid for the academic year in which they are made. Objective tests may include short-answer questions and / or test, problem solving on paper or circuit design with the ISE software. Final grade The final grade is usually calculated as: Final grade = 0.4 x objective test 1 grade + 0.5 x objective test 2 grade + 0,1 x objective test 3 grade Those students who do not have qualification in some of the objective test, or to resort very low scores can choose to make the 3rd objective test with a weight of 100% (the test will be different in this case). So in this case the final grade will be the the qualification of this test. Second opportunity The second time, an objective test that can consist of theoretical and practical questions, written exercises, issues and circuit design with the ISE software will be performed.

Sources of information	
Basic	- Wakerly, John F. (2005). Diseño digital : principios y prácticas. México : Pearson Educación - Tocci, Ronald J. (2007). Sistemas digitales : principios y aplicaciones. México : Prentice Hall - Alvarez Ruiz de Ojeda, Jacobo (2004). Diseño digital con lógica programable. Santiago de Compostela: Tórculo
Complementary	- García Zubía, Javier (2003). Problemas resueltos de electrónica digital. Madrid:Thomson

Recommendations
Subjects that it is recommended to have taken before
Computer Science/770G01002 Fundamentals of Electricity/770G01013 Fundamentals of Electronic Circuits/770G01018
Subjects that are recommended to be taken simultaneously
Subjects that continue the syllabus
Digital Systems I/770G01026
Other comments

(*)The teaching guide is the document in which the URV publishes the information about all its courses. It is a public document and cannot be modified. Only in exceptional cases can it be revised by the competent agent or duly revised so that it is in line with current legislation.