Teaching Guide				
Identifying Data				2020/21
Subject (*)	Digital Systems I		Code	770G01026
Study programme	Grao en Enxeñaría Electrónica Industrial e Automática			
Descriptors				
Cycle	Period	Year	Type	Credits
Graduate	2nd four-month period	Third	Obligatory	6
Language	Spanish			
Teaching method	Face-to-face			
Prerequisites				
Department	Enxeñaría Industrial			
Coordinador	Jove Pérez, Esteban	E-mail	esteban.jove@udc.es	
Lecturers	Jove Pérez, Esteban Meizoso López, Maria del Carmen Zayas Gato, Francisco	E-mail	esteban.jove@udc.es carmen.meizoso@udc.es f.zayas.gato@udc.es	
Web				
General description	O obxectivo desta materia é que o alumno coñeza as memorias e os dispositivos lóxicos programables, así como os métodos e ferramentas de deseño de circuítos sobre dispositivos lóxicos programables.			
Contingency plan	1. Modifications to the contents 2. Methodologies *Teaching methodologies that are maintained *Teaching methodologies that are modified 3. Mechanisms for personalized attention to students 4. Modifications in the evaluation *Evaluation observations: 5. Modifications to the bibliography or webgraphy			

Study programme competences / results	
Code	Study programme competences / results
A26	Coñecer os fundamentos e aplicacións da electrónica dixital e microprocesadores.
A30	Coñecer e ser capaz de modelar e simular sistemas.
A31	Coñecementos de regulación automática e técnicas de control e a súa aplicación á automatización industrial.
B1	Capacidade de resolver problemas con iniciativa, toma de decisións, creatividade e razoamento crítico.
B2	Capacidade de comunicar e transmitir coñecementos, habilidades e destrezas no campo da enxeñaría industrial.
B3	Capacidade de traballar nun contorno multilingüe e multidisciplinar.
B4	Capacidade de traballar e aprender de forma autónoma e con iniciativa.
B5	Capacidade para empregar as técnicas, habilidades e ferramentas da enxeñaría necesarias para a práctica desta.
B6	Capacidade de usar adecuadamente os recursos de información e aplicar as tecnoloxías da información e as comunicacións na enxeñaría.
B7	Capacidade para traballar de forma colaborativa e de motivar un grupo de traballo.
B11	CB4 - Que los estudiantes puedan transmitir información, ideas, problemas y soluciones a un público tanto especializado como no especializado.

C2	Utilizar as ferramentas básicas das tecnoloxías da información e as comunicacións (TIC) necesarias para o exercicio da súa profesión e para a aprendizaxe ao longo da súa vida.
C5	Valorar criticamente o coñecemento, a tecnoloxía e a información dispoñible para resolver os problemas cos que deben enfrontarse.

Learning outcomes			
Learning outcomes	Study programme competences / results		
Programa dispositivos lóxicos programables e configurables e utiliza con soltura a suas ferramentas de desarrollo.	A26 A30	B1 B3	C2
Coñece a realización electrónica dos circuitos convertidores A/D y D/A e sabe elegir o máis adecuado en cada aplicación.	A26 A30	B1 B2 B5 B6	C2 C5
Distingue os tipos de circuitos lóxicos programables e dispositivos de memoria.	A26 A30 A31	B1 B5	C2 C5
Coñece as técnicas de conexión de periféricos básicos, deseña o seus circuitos.	A26 A30	B2 B4 B7 B11	C2 C5

Contents	
Topic	Sub-topic
Contidos da memoria de verificación relacionados cos temas da asignatura	· Programación básica en VHDL: Temas 1 e 2. · Deseño con dispositivos electrónicos configurables CPLD e FPGA: Temas 3, 4 e 6. · Circuitos de memoria. Temas 5, 6 y 7. · Conversión A/D y D/A. Tema 6 e 9. · Ferramentas de deseño e desenvolvemento de sistemas lóxicos programables: Temas 4, 6, 8, 9 e 10. · Transmisión de datos. Temas 8 y 10.
Subject 1. Sequential syncronous systems design	Finite state machines. Analysis and synthesis . VHDL description.
Subject 2. Introduction to Programmable Logic	Programmable circuits features. Steps of design. Aplications.
Subject 3. PLD CoolRunner II architecture	Function Blocks. Macrocells. I/O Blocks. Timming model.
Subject 4. Digital systems design with CPLDs.	Synthesis: Examples of macros codes. Synthesis Report. Options. Translate. Fit:Options. Timming report Secuencial systems design: Clock signals. Synchronous circuits design:counters, control circuits, asynchornous inputs, metaestability. Interface between synchronous systems and other circuits. Design of complex systems: Method and practical application.
Subject 5. Architecture of the FPGAs of the family Spartan 3 E of Xilinx	Logic resources.CLB. Internal memories. Clock Circuits. Multipliers. E/S technologies.
Subject 6. Synchronous design with FPGAs	Synchronous design methodology.
Subject 7: Working with files	File declaration. Reading and writing files. Open and close files. Package std_logic_textio. Examples.
Tema 8. Diseño de un controlador VGA	DA converter for VGA into the Nexys 2. Standard VGA. Controller design.

Subject 8. Design of arithmetic systems with programmable logic	Adders. Subtracters. Multipliers. Dividers
Subject 9. Techniques for improving the performance of syncronous systems.	Duplicating states. Pipelining.

Planning				
Methodologies / tests	Competencies / Results	Teaching hours (in-person & virtual)	Student?s personal work hours	Total hours
Guest lecture / keynote speech	A26	21	0	21
Laboratory practice	B7 B11 C2 C5	30	0	30
Supervised projects	A26 A30 A31 B1 B2 B3 B4 B5 B6	0	85	85
Mixed objective/subjective test	A26 A30 B1	4	0	4
Personalized attention		10	0	10
(*)The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.				

Methodologies	
Methodologies	Description
Guest lecture / keynote speech	Exposición oral e mediante o uso de medios audiovisuais.
Laboratory practice	Desenrolo de prácticas de aplicación dos coñecementos teóricos adquiridos. Manexo do software de simulación e deseño de circuitos dixitais.
Supervised projects	Traballos de realización individual ou en grupo para o deseño dun circuito de complexidade media.
Mixed objective/subjective test	Probas de evaluación que poderán incluir preguntas sobre dos contidos teóricos da asignatura, así como exercicios ou problemas relacionados cos seus contidos.

Personalized attention	
Methodologies	Description
Supervised projects Guest lecture / keynote speech Laboratory practice	Os profesores atenderán persoalmente as dúbidas sobre calquera das actividades desenvolvidas ao longo do curso. O horario de tutorías será publicado ao comezo do cuadrimestre na páxina web do centro. O alumnado con recoñecemento de dedicación a tempo parcial e dispensa académica de exención de asistencia, poderá realizar sesión periódicas co coordinador da materia a través de Microsoft Teams ou correo electrónico.

Assessment			
Methodologies	Competencies / Results	Description	**Qualification**
Supervised projects	A26 A30 A31 B1 B2 B3 B4 B5 B6	Work designing a digital system of medium complexity. The correct application of theoretical concepts to the work performed will be evaluated. It is necessary to submit an explanatory report, make an oral presentation and answer correctly the questions made by the teachers.	40

Mixed objective/subjective test	A26 A30 B1	There will be 2 objective tests to be performed individually for each student. The first will take place once explained the first 5 issues. It will mean the 30% of the final grade. The second test will be the final exam 1st opportunity and can have the following weights: - 30% for those students who decide to do the test of the second part. - 60% for those students who decide to do the test of the first and second parts. In that case, the grade obtained in the first objective test is discarded.	60
Others			

Assessment comments
The scores for the evaluable tasks are only valid for the academic year in which they are made. Objective tests may include short-answer questions and / or test, problem solving on paper or circuit design with the ISE software. To achieve maximum grade at project, the following issues will be considered: - The designed circuits must work perfectly in all its aspects (functional and temporal simulation). - The documentation and presentation must be clear. - The students must explain the reasons to make the design and answer correctly the questions made by the teacher regarding the project. Final grade The final grade is usually calculated as: Final grade = 0.3 x objective test 1 grade + 0.4 x project grade + 0,3 x objective test 2 grade Those students who do not have qualification in the 1st objective test, or, to resort very low scores can choose to make the 2nd objective test (the test will be different in this case). In this case the final grade will be: Final grade= 0.4 x project grade + 0,6 x objective test 2 grade Second opportunity The second time, an objective test that can consist of theoretical and practical questions, written exercises, issues and implementation of a circuit in one of the Laboratory boards will be performed.

Sources of information	
Basic	- Jacobo Álvarez Ruiz de Ojeda (2004). Diseño Digital con Lógica Programable. Santiago de Compostela. Tórculo - Jacobo Álvarez Ruiz de Ojeda (2012). Diseño digital con FPGAs. Madrid : Vision Ebooks
Complementary	- Roy W. Goody (2001). OrCAD PSpice for Windows. Prentice Hall - Tocci. Ronald J. (1996). Sistemas Digitales. Prentice Hall

Recommendations
Subjects that it is recommended to have taken before
Fundamentals of Electricity/770G01013 Fundamentals of Electronic Circuits/770G01018 Analog Electronics/770G01022 Digital Electronics/770G01023
Subjects that are recommended to be taken simultaneously
Subjects that continue the syllabus
Digital Systems II/770G01034
Other comments

Nesta asignatura dase por suposto que o alumno sabe programar en linguaxe VHDL, e manexa o entorno de deseño ISE Web Pack de Xilinx, polo que para matricularse con posibilidades de éxito é preciso haber cursado con aproveitamento Electrónica Dixital, ou ben haber adquirido esos coñecementos previamente.